Description

A METHOD, APPARATUS AND CIRCUIT FOR LATCHUP SUPPRESSION IN A GATE-ARRAY ASIC ENVIRONMENT

BACKGROUND OF INVENTION

[0001] FIELD OF THE INVENTION

[0002] The present invention generally relates to latchup suppression integrated circuits, and more particularly to providing latchup suppression in a gate-array ASIC environment.

[0003] BACKGROUND OF THE INVENTION

[0004] As the internal structures in integrated circuits are getting smaller, it is getting more difficult to control the phenomenon known as "latchup." Latchup occurs when a pnpn structure transitions from a low current high voltage state to a high current low voltage state through a negative resistance region (i.e., forming an S-Type I-V (current/voltage) characteristic). Latchup is an unwanted phenomenon in that it either completely destroys or severely impairs electronic components within an integrated circuit.

[0005] Latchup is typically understood as occurring within a pnpn structure, or silicon controlled rectifier (SCR) structure. Interestingly, pnpn structures may be both intentionally designed and unintentionally formed between

structures. Hence, latchup conditions may occur within peripheral circuits or internal circuits, within one circuit (intra-circuit), or between multiple circuits (inter-circuit).

[0006] Latchup is typically initiated by an equivalent circuit of a cross-coupled pnp and npn transistor. With the base and collector regions being cross-coupled, current flows from one device leading to the initiation of the second device ("regenerative feedback"). These pnp and npn elements may be any diffusions or implanted regions of other circuit elements (e.g., p-channel MOSFETs, n-channel MOSFETs, resistors, etc.) or actual pnp and npn bipolar transistors. In CMOS, the pnpn structure may be formed with a p-diffusion in a n-well, and a n-diffusion in a p-substrate ("parasitic pnpn"). In this case, the well and substrate regions are inherently involved in the latchup current exchange between regions.

[0007] The condition for triggering a latchup is a function of the current gain of the pnp and npn transistors, and the resistance between the emitter and the base regions. This inherently involves the well and substrate regions. The likelihood or sensitivity of a particular pnpn structure to latchup is a function of spacings (e.g., base width of the npn and base width of the pnp), current gain of the transistors, substrate resistance and spacings, the well resistance and spacings, and isolation regions.

[0008] Latchup is a concern in both internal circuits and peripheral circuitry. Latchup may also occur as the result of interaction of the ESD device, the I/O off-chip driver, and adjacent circuitry initiated in the substrate from overshoot and undershoot phenomenon. These may be generated by CMOS off-chip driver

circuitry, receiver networks, and electrostatic discharge (ESD) devices. In CMOS I/O circuitry, undershoot and overshoot may lead to injection in the substrate. Hence, both a p-channel MOSFET and an n-channel MOSFET may lead to substrate injection. Simultaneous switching of circuitry, where overshoot or undershoot injection occurs, leads to injection into the substrate which leads to both noise injection and latchup conditions. Supporting elements in these circuits, such as pass transistors, resistor elements, test functions, over voltage dielectric limiting circuitry, bleed resistors, keeper networks, and other elements may be present leading to injection into the substrate. ESD elements connected to the input pad may also lead to latchup. ESD elements that may lead to noise injection and latchup include MOSFETs, pnpn SCR ESD structures, p+/n-well diodes, n-well-to-substrate diodes, n+ diffusion diodes, and other ESD circuits. ESD circuits may contribute to noise injection into the substrate and latchup.

[0009] An additional process may occur by the interaction of "activated" and "unactivated" elements in a gate-array environment. In an ASIC environment, a "sea of gates" philosophy allows customization and personalization of circuit elements at a metalization level where the silicon regions are predefined. Unused n-diffusion regions are grounded, and unused p-diffusion regions are connected to V_{DD}. Unfortunately, this implementation may lead to latchup. As the substrate voltage potential rises relative to the n-diffusion, all the elements of the gate arrays tend to forward bias. As the substrate voltage potential lowers, the unused p-diffusion elements, the n-well and the substrate may activate the vertical pnp. This may occur as a result of minority carrier injection in wells and substrate regions.

[0010] In an ASIC gate array environment, it has been observed that as a negative pulse is injected into an input pad, ESD current discharge to the substrate may flow outside of the I/O cell region, leading to "turn-on" of the adjacent gate array regions connected to the V_{SS} and V_{DD} rails. This often results in increasing the likelihood of latchup and leading to failure of the latchup specification.

[0011] An additional problem in latchup is the propagation of the latchup process once latchup is initiated in an array environment. As an initial source injects electrons into the substrate, a first circuit element may latchup. The latchup of a first circuit leads to the turn-on of a pnp parasitic element leading to more injection into the substrate. As a result, the injection into the substrate of the primary initial perturbation is additive by linearity to the secondary injection initiated by the circuit undergoing latchup. This leads to an adjacent circuit to also latchup as the total current of the initial primary injection current (which decreases with distance from initial injection point) is additive to the secondary. This leads to a propagation run-away effect leading to additional latchup propagation. Hence, the solution of detachment of the rails is a structure to "truncate the latchup propagation" through the semiconductor chip and array region.

[0012] Latchup may be initiated by negative transient on the V_{DD} which may lead to a forward biasing of all the n-diffusions and n-well structures and electron injection throughout the semiconductor chip substrate. This produces a "sea of electrons" injected in the chip substrate. Equivalently, a positive transient on the V_{SS} may lead to hole injection and forward biasing of the substrate-well junction providing a "sea of holes" event. In this event, it is

possible the metric of how far the detachment is placed may be dependent on other physical parameters, such as the latchup sensitivity of the gate array element, circuit type (e.g., SRAM cell, logic gate, gate array MOSFET) based on the parasitic current gains, substrate, and well resistances.

[0013] Latchup may occur from voltage or current pulses that occur on the power supply lines, such as V_{DD} and V_{SS}. Transient pulses on power rails (e.g., substrate or wells) may trigger latchup processes. The propagation of the impulse on the power grids may also be quantified and appropriate latchup control networks may be placed. Latchup may also occur from a stimulus to the well or substrate external to the region of the thyristor structure from minority carriers.

[0014] Latchup may be initiated from internal or external stimulus. Latchup is known to occur from single event upsets (SEU). Single event upsets may include terrestial emissions from nuclear processes, cosmic ray events, as well as events in space environments. Cosmic ray particles may include proton, and neutron, gamma events, as well as a number of particles that enter the earth atmosphere. Terrestial emissions from radioactive events, such as alpha particles, and other radioactive decay emissions, may also lead to latchup in semiconductors. In this case, it is possible that the methodology is applied to sensitive gate array circuits, as well as other circuits, such as pass transistors and SRAM cells. As applied to the gate array circuits, the SRAM power rails and ground rails may be decoupled to avoid latchup or SEU events. In this case, the methodology may be addressed by certain functional blocks instead of spatial dependence. Hence the methodology of detachment and connection to the latchup control networks may be

according to the circuit type as well as physical localness (placement) to the injection source.

SUMMARY OF INVENTION

[0015] The present invention is a method and apparatus for improving the latchup tolerance of circuits embedded in an integrated circuit while avoiding direct electrical connection to power rails using circuit implementations for gate array environments.

[0016] One aspect of the invention is an integrated circuit having a substrate, a power rail, a sea of gates, and a latchup control isolation network electrically coupled to the substrate. The latchup control isolation network electrically isolates the sea of gates from the power rail.

[0017] Another aspect of the present invention is an integrated circuit having a substrate, a power rail, a sea of gates, and an active clamp network electrically coupled to the substrate. The active clamp network electrically isolates the sea of gates from the power rail.

[0018] Still another aspect of the present invention is a method of suppressing latchup in an integrated circuit in a substrate, the circuit having a sea of gates and a power rail. The method includes the following steps: electrically connecting a latchup control isolation network or an active clamp network to the substrate; and if the latchup control isolation network is electrically connected to the substrate, turning off the latchup control isolation network or if the active clamp network is electrically connected to the substrate turning on the active clamp network thereby isolating the power rail from the

sea of gates.

[0019] Other features, utilities and advantages of various embodiments of the invention will be apparent from the following more particular description of embodiments of the invention as illustrated in the accompanying drawings.

BRIEF DESCRIPTION OF DRAWINGS

[0020] The foregoing and other objects, aspects and advantages will be better understood from the following detailed description of a preferred embodiment of the invention with reference to the drawings, in which:

[0021] FIG. 1 is a schematic partial cross-sectional view of a prior art parasitic latchup structure environment highlighting a gate array interacting with an ESD, I/O or integrated circuit;

[0022] FIG. 2 is a schematic partial cross-sectional view of a cross section of a parasitic latchup structure highlighting a gate array and an integrated circuit solution according to one embodiment of the present invention;

[0023] FIG. 3 is a schematic partial cross-sectional view of one embodiment according to the present invention;

[0024] FIG. 4 is a schematic partial cross-sectional view of one embodiment according to the present invention;

[0025] FIG. 5 is a schematic partial cross-sectional view of one embodiment according to the present invention;

[0026] FIG. 6 is a layout schematic of one embodiment according to the the present

invention; and

[0027] FIG. 7 is a block diagram of methodology according to one embodiment of the present invention.

DETAILED DESCRIPTION

[0028] The present invention is an integrated circuit device and related method for improving the latchup tolerance of circuits by avoiding direct electrical connection to power rails when using circuit implementations including gate array environments.

[0029] Referring to FIG. 1, a cross-section view of a portion of a semiconductor chip substrate 10 illustrates a gate array structure environment 12 (also referred to as gate array 12 herein) in an integrated circuit. Substrate 10 includes an n-well region 14 with a well contact 16. N-channel MOSFET 17 of gate array 12 is connected to V_{SS} power rail 18. P-channel MOSFETs 19 of gate array 12 are connected to a V_{DD} rail 20.

[0030] N-well region 14 may represent a diffused well, a retrograde well, a subcollector, or other vertical modulated wells. Substrate 10 may represent a p-well, a p- epi/p+ substrate, a p- wafer with a p+ buried layer, or other known substrate doping profiles.

[0031] Substrate 10 supports the integrated electronics of the integrated circuit. Located within n-well region 14 are p-doped regions 22 that form part of p-channel MOSFETs 19. Also located within substrate 10 are n-doped regions 24 that form part of n-channel MOSFETs 17. Substrate 10 also includes a substrate contact 26. It should also be noted that power (V_{DD})

and ground (V_{SS}) are applied to well contact 16 and substrate contact 26, respectively.

[0032] The structure illustrated in FIG. 1 demonstrates the ease with which a parasitic pnpn structure may be formed in either a CMOS or BiCMOS technology from the p-doped regions 22, the n-well 14, substrate 10 and n-doped regions 24. The parasitic pnpn structure may cause undesirable latchup region problems. In a gate array environment, as the substrate voltage potential increases, the n-diffusions of the MOSFET gate array forward bias discharging current to the V_{SS} power rail. Additionally, a negative bias of the V_{SS} substrate may lead to a forward active state of a vertical pnp.

[0033] In the above configuration, where there are connections directly to the power grid, current is able to leave the area of the I/O or ESD circuit in which it is generated and is injected into the power domain (e.g., V_{SS} or V_{DD}) of the chip. Furthermore, allowing the injection into substrate 10 or n-well region 14 may initiate a latchup state. For example, if n-doped regions 24 are grounded and a positive pulse is applied to p-doped regions 22, latchup may occur. In further example, negative pulses may initiate a latchup between regions. In addition, a negative undershoot on substrate 10 may lead to latchup.

[0034] Referring now to FIG. 2, where like elements in FIGS. 1 and 2 are indicated by like element numbers in FIG. 2, a cross-section illustrates an embodiment of an integrated circuit structure of the present invention, which is designed to counteract parasitic latchup. In FIG. 2, the n-diffusions (not illustrated) of

n-channel MOSFETs 17 of gate array 12 are isolated from V_{SS} power rail 18 with circuit elements 30 and 32 to prevent the forward biasing of substrate 10 relative to the n-diffusions from occurring. Equivalently, circuit elements 34 and 36 prevent p-channel MOSFETs 19 from discharging from V_{DD} rail 20. P-doped region 22 is connected to circuit element 36 instead of directly to power supply voltage V_{DD} 20. In FIG. 2, circuit element 34 is an inverter circuit whose input is connected to n-well contact 16, and whose output is connected to gate 38 of MOSFET element 36. In FIG. 2, n-doped region 24 is connected to circuit element 32. Circuit element 32 is located between the source and drain of MOSFET 17 and substrate power rail V_{SS} 18. Substrate contact 26 is connected to circuit element 30. In FIG. 2, circuit element 30 is an inverter circuit whose input is connected to substrate contact 26, and whose output is connected to gate 40 of element 32.

[0035] In the embodiment illustrated in FIG. 2, perturbations to the well or substrate voltage potential are sensed by well and substrate contacts 16 and 26. This perturbation signal is then sensed on inverter circuit 30 (referred to as element 30 previously). When a perturbation signal is undesirable, leading to a latchup event, elements 30 and 32 or 34 and 36 isolate the p-channel or n-channel gate array elements, respectively, from the respective power supply rails.

[0036] Still referring to FIG. 2, substrate contact 26, a p+ type contact, is located local to substrate 10. Substrate contact 26 is then connected to a gate (not illustrated) of inverter circuit 30. As the p+ substrate contact 26 connected locally increases in potential, the output signal of inverter circuit 30 is lower. The output of inverter circuit 30 is connected to gate 40, of MOSFET circuit

element 32, which functions as a gate-array latchup control element. MOSFET element 32 has a source 41 that is connected to the n+ regions 24 of MOSFET 17 of gate array 12. MOSFET element 32 is connected to V_{SS}. As the substrate voltage potential rises, source 41 of MOSFET circuit element 32 is turned off at its threshold voltage. The threshold voltage is a predetermined value. This then allows substrate 10 to be decoupled from VSS rail 18 and allows the diffusions to float when the substrate voltage potential inadvertently rises as a result of poor substrate grounding and injection of minority carriers. An equivalent circuit may be initiated for the p-doped regions 22 to decouple the p-doped regions and n-well contact 16 from V_{DD} power supply 20.

[0037] Referring now to FIG. 3 where like elements between FIG. 3 and previous FIGS. are represented by like element numbers in FIG. 3, in another embodiment, active clamp networks 50 and 52 may be used in place of inverter circuit elements 30 and 34, respectively, in the embodiment illustrated in FIG. 2. As the V_{DD} or V_{SS} potential goes beyond the normal functional regime, active clamp networks 50 and 52 isolate V_{SS} rail 18 from n-channel MOSFETs 17 and for a second state and isolates V_{DD} rail 20 from the p-channel MOSFETs 19.

[0038] Active clamp networks generally have the advantage of being able to respond at any excursion outside the normal operational regime. While diode based implementations respond to excursions greater than or equal to V_{DD} $+V_{be}$, V_{be} being the forward bias voltage of a junction, active clamp networks may respond to excursions greater than or equal to the V_{DD} power supply voltage. Additionally, active clamp networks may also respond to

voltage excursions below V_{SS}, instead of below V_{SS} -V_{be} as in diode-based schemes. An active clamp network is designed utilizing a reference control network. This may also be referred to as a pseudo-zero VT pass transistor element.

[0039] A reference control network is used where the reference potential is set to V_{tn}, and a second reference control network is used whose reference potential is V_{DD} -V_{tp}. These references may be established using a MOSFET whose gate is coupled to its own drain connection. The network is established where a second NFET has its gate connected to reference V_{tn}. The network is established where a second PFET has its gate connected to a reference V_{DD} -V_{tp}. These control elements sense the V_{DD} and substrate local potential. When the local substrate connection or the local well connection fall outside of the normal voltage range, these elements "turn on." The turn-on of these elements lead to the turning off of a transistor element between the gate array diffusions and corresponding power supplies. In the embodiment, as the substrate voltage potential increases, the signal goes below substrate (e.g., zero potential). V_{DD}, V_{be}, V_{SS}, and V_{tp} may all be predetermined values.

[0040] Referring now to FIG. 4, another embodiment of an active clamp type network is illustrated. In FIG. 4, the active clamp type network includes a substrate contact 60, an inverter circuit 62, a reference control network 64, a MOSFET switch device 66, a diode 68, and a pad 70. Reference control network 64 includes a MOSFET 71 having a source 72 connected to V_{DD} 74, and a gate (not shown) connected to its drain 76, forming a potential at V_{DD} - V_{tp}. When an excursion occurs in substrate 10 below pad 70, the

current will flow from the pad to power rail V_{SS} 78 when the pad goes below zero volts. In this case, reference control network 64 insures turn-on at the zero volt potential forming a pseudo-zero VT response. This prevents negative current injection into substrate 10 and eliminates noise injection to the substrate. When substrate 10 rises from a positive discharge or response, the signal is inverted by inverter circuit 62, turning on MOSFET switch 66. As a result, reference control network 64 addresses both an active clamp for negative excursions at pad 70, and a positive excursion from an increase in the substrate voltage potential.

[0041] FIG. 5 illustrates an embodiment which utilizes the pseudo-zero VT concept for perturbations of the substrate voltage potential local to the gate array implementation. In FIG. 5, the structure and circuit consists of a substrate 10, a p+ substrate contact 80, an inverter circuit 82, a pseudo-zero VT pass transistor 84, a gate reference control network 86, a switch 88, and a gate array element 90. The gate 96 of pass transistor 84 is connected to reference control network 86 that establishes a potential. The reference control voltage is V_{DD} -V_{tp}. Other embodiments to establish this potential may be established using resistor divider networks, capacitive dividers, or other configurations known to those skilled in the art for providing the voltage potential that is desired. When the potential at p+ contact 80 decreases below zero, the pseudo-zero VT half pass, transistor 84 will turn on, pulling down the gate of switch device 88, thereby isolating gate array element 90 from power supply connection V_{SS} 98. An equivalent circuit may be established for the p-channel MOSFET gate array network elements, corresponding V_{DD} supply 100, and reference control network 86 set at V_{tn}.

[0042] In FIG. 6, an example of one embodiment of the present invention is illustrated. The gate array latchup control network is constructed local to the gate array itself or in a service module along a plurality of I/O elements. In this example, the structure includes an I/O network, an ESD device, a gate array, and a gate-array latchup control network.

[0043] The structure includes a gate array 110 of n-channel and p-channel MOSFET transistors joined to a latchup control function 112 contained in a service module 114 via electrical connections 116. I/O cell MOSFETs 118 and ESD elements 120 are contained in peripheral circuits 122 of the semiconductor chips. Service module 114 may contain other circuit function and logic 124. The substrate contacts and well contacts (not illustrated) are local to the gate array elements as shown in FIGS. 1-5. Electrical connections of the latchup control networks, references, and other support circuit may be placed in (consistent terminology) service module 114 to provide the necessary controls for the bank of gate arrays adjacent or local to I/O and ESD elements 118 and 120.

[0044] As the substrate and well potentials are disturbed from the I/O or ESD cell injection, the substrate sensing may decouple gate array elements 110 according to the embodiments illustrated in FIGS. 2-5.

[0045] In FIG. 7, a block diagram illustrates the steps of a method according to one embodiment of the present invention. The system illustrated in FIG. 7 includes a methodology that allows for the customization of the "sea of gates" by disconnection of the n-regions from the gate array latchup control network as these elements are utilized in circuits. Such a methodology may

include forming a sea of gates, forming a latchup gate array control network, forming a ESD network, forming a I/O cell, and providing a means of isolating said gates from said latchup gate array control network for personalization and customization of an integrated circuit.

[0046] As illustrated in FIG. 7, in the system's first step 130, the gate array circuit is identified and established. When the gate array region is identified, the source, drain and gate are separated from the power supplies is established at step 132. Then, the electrical connections which are directly connected to the V_{DD} or V_{SS} may be connected to the latchup control circuit at step 134. Finally, at step 136, the circuit electrical connections are established.

[0047] Typically, only elements close to the substrate or well injection are decoupled from the V_{DD} and V_{SS} power supplies. Regions of the semiconductor chip far from injection sources may not require isolation of these elements to avoid latchup. Minority carrier injections may diffuse from the injection source location, providing potential disturbances and injection into the substrate or n-well regions and initiating latchup. In this case, as part of the system illustrated in FIG. 7, a distance is defined based on known injection source regions. For example, the decoupling of the gate array elements may be applied to gate array elements from a certain distance from the injection source. In chip design, the injection sources (e.g., I/O cell and ESD elements) may be defined according to the relative distance from these elements to the latchup prone elements. The detachment of the source, drain, and gate electrodes may be applied to a certain distance. From the known size of the injection source input, and relative placement, the magnitude of the current and potential may be determined at the gate array

element. In this manner, a heuristic or metric may be defined to decide how far the method of detachment is applied and which gate array block items are reconnected to the latchup control circuitry function. For example, electron recombination is a function of the electron diffusion length. The electron diffusion length is dependent on the diffusion coefficient and the electron recombination time. The electron recombination time is inversely proportional to the doping concentration of the substrate.

[0048] While the present invention has been described in connection with specified embodiments, it will be understood that it is not so limited. On the contrary, it is intended to cover all alternatives, modifications and equivalents as may be included within the spirit and scope of the invention as defined in the appended claims.